Page 11, line 17, after "between" insert --the remainder of etched structure 152, which is also referred to herein as--;

Page 11, line 17, replace "defining" with --and which defines--;

Page 11, line 17, after "mesas" insert --152--;

Page 11, line 17, after "ridges" insert --152--;

Page 11, line 21, change "FIG.24" to --FIG. 24--.

IN THE ABSTRACT:

On page 22, line 6, change "upper most" to --uppermost--;

On page 22, line 7, insert a comma after "etched".

IN THE CLAIMS:

16. (Amended) A storage poly structure for a semiconductor capacitor, said storage poly structure including recesses formed therein and having a hemispherical-grain polysilicon layer thereon and a mask over the hemispherical-grain polysilicon layer, portions of the hemispherical-grain polysilicon layer being exposed through said mask, said storage poly structure formed by the method comprising:

providing a storage poly structure;

growing the [a] hemispherical-grain polysilicon layer on said storage poly structure;

applying the [a] mask [layer] over said hemispherical-grain polysilicon layer;

removing an upper portion of [said] the mask [layer] to expose elevated portions of [said] the hemispherical-grain polysilicon layer; and

etching through said exposed portions of said hemispherical-grain polysilicon layer [portions] and into said storage poly structure so as to form the recesses in said storage poly structure.

17. (Amended) The storage poly structure of claim 16, wherein the method further [comprising] comprises:

depositing a photo-resist material on said storage poly structure to pattern [a desired position] at least a portion of said storage poly structure;

etching said storage poly structure; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

B4 Cont

18. (Amended) The storage poly structure of claim 16, wherein said providing [a] said storage poly structure comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are [position in desired areas for] positioned so as to facilitate formation of said storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer down to [the] said barrier layer[forming said storage poly].

19. (Amended) The storage poly structure of claim 18, wherein said planarizing is performed using a mechanical abrasion.

B5

21. (Amended) A semiconductor capacitor including a storage poly structure with recesses formed therein, a hemispherical-grain polysilicon layer on the storage poly structure, and dielectric material at least lining the recesses, said semiconductor capacitor produced by the method comprising:

providing the storage poly structure;

growing [a] the hemispherical-grain polysilicon layer on [said] the storage poly structure;

applying a mask layer over [said] the hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of [said] the hemispherical-grain polysilicon layer;

etching through said exposed portions of [said] the hemispherical grain polysilicon layer [portions] and into [said] the storage poly structure so as to form the recesses in the storage poly structure;

depositing [a] dielectric material over said etched storage poly structure so as to at least line the recesses; and

depositing a cell poly over said dielectric material.

22. (Amended) The semiconductor capacitor of claim 21, wherein said method further [comprising] comprises:

depositing a photo-resist material on said storage poly structure to pattern [a desired position] at least a portion of [said] the storage poly structure;

etching [said] the storage poly structure; and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

23. (Amended) The semiconductor capacitor of claim 21, wherein said providing [a] the storage poly comprises:

depositing a buffer layer on a semiconductor substrate;

patterning a resist material on said buffer layer wherein open areas in said resist material are [position in desired areas for] positioned so as to facilitate formation of [said] the storage poly structure;

etching said buffer layer to expose portions of said semiconductor substrate;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer to the barrier layer forming [said] the storage poly structure.

B5 Cont'd

24. (Amended) The semiconductor capacitor of claim 23, wherein said planarizing is performed using a mechanical abrasion.

B6

26. (Amended) A semiconductor memory cell including a storage poly structure with recesses formed therein, a hemispherical-grain polysilicon layer on the storage poly structure, and dielectric material at least lining the recesses, said semiconductor memory cell produced by a method comprising:

providing an intermediate structure comprising a semiconductor substrate including at least one field oxide area and at least one active area containing at least one drain region and at least one source region, at least one transistor gate member residing on said substrate active area spanned between said at least one drain region and said at least one source region, and [a] the storage poly structure, which is in contact with the semiconductor substrate;

growing [a] the hemispherical-grain polysilicon layer on [said] the storage poly structure;

applying a mask layer over [said] the hemispherical-grain polysilicon layer;

removing an upper portion of said mask layer to expose elevated portions of [said] the hemispherical-grain polysilicon layer;

etching through said exposed portions of [said] the hemispherical grain polysilicon layer [portions] and into said storage poly structure so as to form the recesses in said storage poly structure;

depositing [a] dielectric material over said etched storage poly structure so as to line the recesses; and

depositing a cell poly over said dielectric material.

27. (Amended) The semiconductor memory cell of claim 26, wherein [said] the storage poly structure of [said] the intermediate structure is formed by:

applying a storage poly layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

depositing a photo-resist material on said storage poly structure to pattern [a desired position of] said storage poly [structure] layer;

[etching said storage poly;] and

removing said photo-resist material prior to etching through said hemispherical grain polysilicon layer exposed portions.

28. (Amended) The semiconductor memory cell of claim 26, wherein [said] the storage poly structure of [said] the intermediate structure is formed by:

B6 depositing a buffer layer over said at least one field oxide area, said at least one active area, and said at least one transistor gate member;

patterning a resist material on said buffer layer wherein open areas in said resist material are [position in desired areas for] positioned so as to facilitate formation of [said] the storage poly structure;

etching said buffer layer to expose at least a portion of said active area;

removing said resist material;

applying a layer of polysilicon over said barrier layer wherein said polysilicon layer contacts said semiconductor substrate; and

planarizing said polysilicon layer down to [the] said barrier layer[forming said storage poly].

29. (Amended) The semiconductor memory cell of claim 28, wherein said planarizing is performed using a mechanical abrasion.

B3 (Amended) 31. (Amended) A semiconductor capacitor storage poly including downwardly extending recesses formed therein, said recesses comprising a plurality of contiguous mesas forming a maze-like structure.

to Amend B2 33. (Amended) A semiconductor capacitor storage poly including downwardly extending recesses formed therein, said recesses comprising a plurality of contiguous webs forming a maze-like structure.

Please add the following new claims:

35. An intermediate semiconductor capacitor structure, comprising:
a storage poly structure with recesses formed therein;
a hemispherical-grain polysilicon layer over said storage poly structure; and
a mask over said hemispherical-grain polysilicon layer, portions of said hemispherical-grain polysilicon layer being exposed through said mask.

36. The intermediate semiconductor capacitor structure of claim 35, wherein said recesses communicate with exposed regions of said hemispherical-grain polysilicon layer.

37. An intermediate semiconductor memory cell structure, comprising:
a storage poly structure with recesses formed therein;
a hemispherical-grain polysilicon layer on said storage poly structure; and
dielectric material at least lining the recesses.

38. A semiconductor memory cell structure, comprising:
a storage poly structure;
a plurality of recesses extending into said storage poly structure; and
and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses.

39. The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over said dielectric layer.

40. The semiconductor memory cell structure of claim 38, wherein said storage poly structure has a web-like structure.

41. The semiconductor memory cell structure of claim 38, wherein at least some of said plurality of recesses extend into said storage poly structure.--